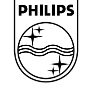
DATA SHEET

TDA4557
Multistandard decoder

Product specification
File under Integrated Circuits, IC02

March 1991

Philips Semiconductors





GENERAL DESCRIPTION

The TDA4557 is a monolithic integrated multistandard colour decoder for the PAL, SECAM, NTSC 3.58 MHz and NTSC 4.43 MHz standards.

FEATURES

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 µs glass delay line
- Chrominance output stage for driving the 64 µs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the demodulators (PAL, NTSC, SECAM)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit and 50/60 Hz recognition
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 13)	V_P	10.8	12.0	13.2	V
Supply current (pin 13)	I_P	–	65	–	mA
Chrominance input voltage					
(peak-to-peak value)	$V_{15(p-p)}$	20	100	400	mV
Chrominance output voltage					
(peak-to-peak value)	$V_{12(p-p)}$	–	1.6	–	V
Colour difference output voltages					
(peak-to-peak values)					
–(R-Y)	$V_{1(p-p)}$	–	1.05 V ± 2 dB	–	V
–(B-Y)	$V_{3(p-p)}$	–	1.33 V ± 2 dB	–	V
Sandcastle pulse (pin 24)					
Required amplitude to separate					
vertical and horizontal pulse	$V_{24(p-p)}$	2.0	2.5	3.0	V
horizontal pulse	$V_{24(p-p)}$	4.1	4.5	4.9	V
burst gating pulse	$V_{24(p-p)}$	7.7	–	V_P	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117); SOT117-1; 1996 November 27.

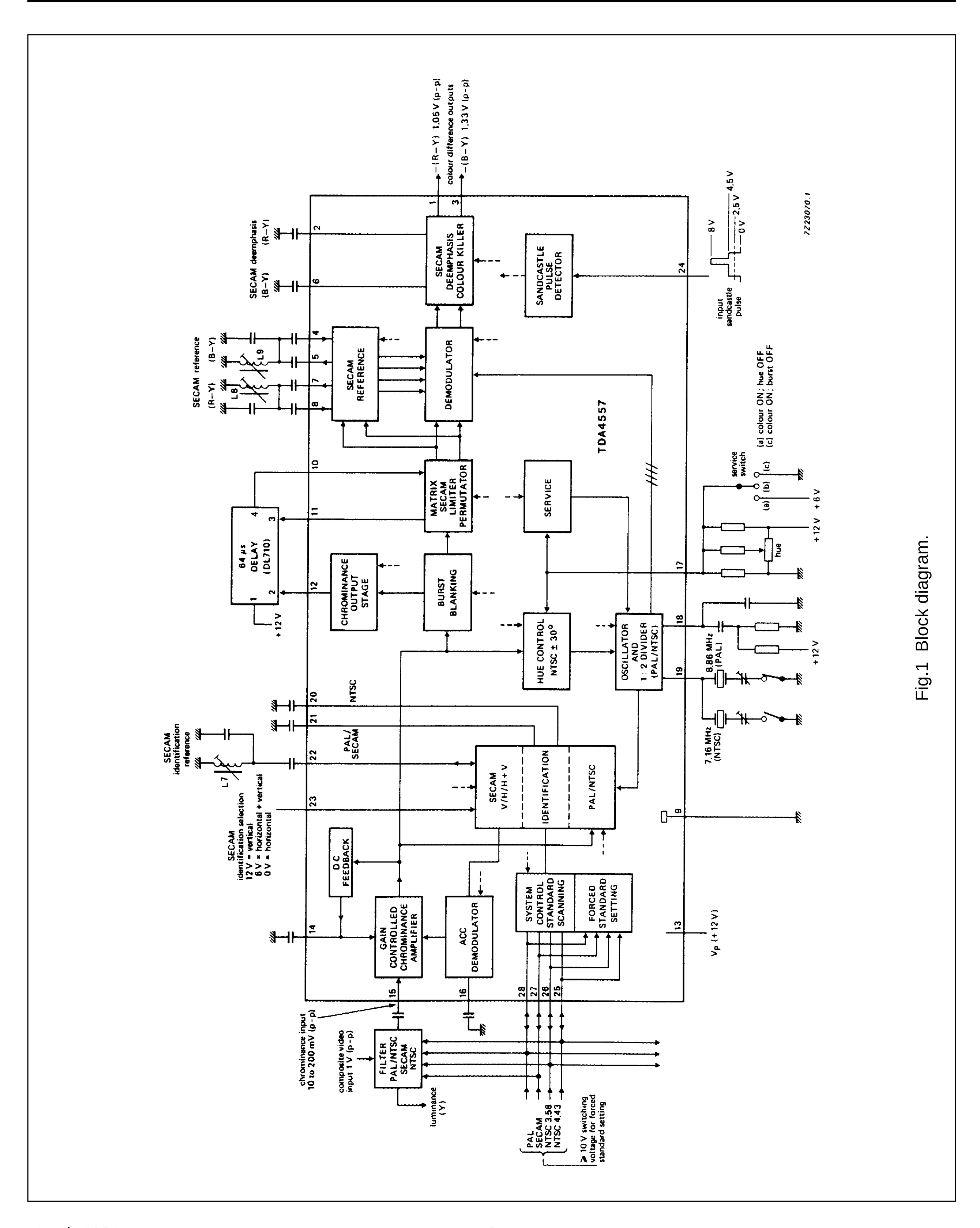


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage (pin 13)	V_P	–	13.2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	V_{n-9}	0	V_P	V
Current at pin 12	I_{12}	–	8	mA
Peak value	I_{12M}	–	15	mA
Total power dissipation	P_{tot}	–	1.4	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig.1; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply (pin 13)					
Supply voltage range	V_P	10.8	1.2	13.2	V
Supply current	I_P	50	65	80	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15(p-p)}$	20	100	400	mV
input impedance	$\lvert Z_{15-9} \rvert$	7	10	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12(p-p)}$	1.1	1.6	1.75	V
output impedance (npn emitter follower)	$\lvert Z_{12-9} \rvert$	–	–	20	Ω
DC output voltage	V_{12-9}	7.3	8.2	9.0	V
Input for delayed signal (pin 10)					
DC input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
– (R-Y) signal (pin 1)	$V_{1(p-p)}$	–	1.05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3(p-p)}$	–	1.33 V ± 2 dB	–	V
Ratio of colour difference output signals					
(R-Y)/(B-Y)	$V_{1/3-9}$	–	0.79 ± 10%	–	
Residual carrier (subcarrier frequency)					
(peak-to-peak value)	$V_{1,3(p-p)}$	–	–	30	mV
Residual carrier (PAL only)					
(peak-to-peak value)	$V_{1,3(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1)					
(peak-to-peak value) without input signal	$V_{1(p-p)}$	–	–	10	mV
DC output voltage					
npn emitter follower with internal current source of 0.3 mA	$V_{1,3-9}$	7.0	7.7	8.4	V
output impedance	$\lvert Z_{1,3-9} \rvert$	–	–	150	Ω

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Demodulator part (SECAM)					
Colour difference signals (see note 3)					
output voltage (proportional to $V_{13\text{-}9}$) (peak-to-peak value)					
–(R-Y) signal (pin 1)	$V_{1(p\text{-}p)}$	–	1.05	–	V
–(B-Y) signal (pin 3)	$V_{3(p\text{-}p)}$	–	1.33	–	V
Ratio of colour difference output signals					
(R-Y)/(B-Y)	$V_{1/3\text{-}9}$	–	0.79 [1] ± 10%	–	
Residual carrier (4 to 5 MHz)					
(peak-to-peak value)	$V_{1,3(p\text{-}p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz)					
(peak-to-peak value)	$V_{1,3(p\text{-}p)}$	–	20	30	mV
H/2 ripple					
at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3(p\text{-}p)}$	–	–	30	mV
DC output voltage	$V_{1,3\text{-}9}$	7.0	7.7	8.4	V
Shift of inserted levels relative to levels					
of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T$(R-Y)	–	0.5	0.6	mV/K
	$\Delta V/\Delta V_P$	–	8	–	mV/V
HUE control (NTSC)/service switch					
Phase shift of reference carrier					
at $V_{17\text{-}9}$ = 2 V	$-\phi$	30	40	–	deg
at $V_{17\text{-}9}$ = 3 V	ϕ	–	0	–	deg
at $V_{17\text{-}9}$ = 4 V	$+\phi$	30	40	–	deg
Input resistance	$R_{17\text{-}9}$	–	5	–	k Ω
Service position					
Switching voltage (pin 17)					
burst OFF; colour ON (for oscillator adjustment)	$V_{17\text{-}9}$	0	–	0.5	V
HUE control OFF; colour ON					
(for forced colour ON)	$V_{17\text{-}9}$	6	–	V_P	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency					
input resistance	$R_{19\text{-}9}$	–	350	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	–	–	Hz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Identification part					
Switching voltages for chrominance filters and crystals					
at pin 28 (PAL)					
at pin 27 (SECAM)					
at pin 26 (NTSC 3.58 MHz)					
at pin 25 (NTSC 4.43 MHz)					
Control voltage OFF state	$V_{25,26,27,28\text{-}9}$	–	–	0.5	V
Control voltage ON state					
during scanning; colour OFF	$V_{25,26,27,28\text{-}9}$	2.1	2.45	2.7	V
colour ON	$V_{25,26,27,28\text{-}9}$	5.5	5.8	6.2	V
Output current	$-I_{25,26,27,28\text{-}9}$	–	–	3	mA
Voltage for forced switching ON					
PAL	$V_{28\text{-}9}$	9	–	V_P	V
SECAM	$V_{27\text{-}9}$	9	–	V_P	V
NTSC 3.58 MHz	$V_{26\text{-}9}$	9	–	V_P	V
NTSC 4.43 MHz	$V_{25\text{-}9}$	9	–	V_P	V
Delay time for					
restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for					
horizontal identification (H)	$V_{23\text{-}9}$	0	–	2	V
vertical identification (V)	$V_{23\text{-}9}$	10	–	V_P	V
combined (H) and (V) identification	$V_{23\text{-}9}$	–	6 (note 2)	–	V
Sequence of standard inquiry					
PAL-SECAM-NTSC 3.58 MHz-NTSC 4.43 MHz					
Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (see note 4)					
Input voltage pulse levels (pin 24)					
to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1.3	1.6	1.9	V
required pulse amplitude	$V_{24(p\text{-}p)}$	2.0	2.5	3.0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3.3	3.6	3.9	V
required pulse amplitude	$V_{24(p\text{-}p)}$	4.1	4.5	4.9	V
to separate burst gating pulse	$V_{24\text{-}9}$	6.6	7.1	7.6	V
required pulse amplitude	$V_{24(p\text{-}p)}$	7.7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1.0	V
Input current	$-I_{24}$	–	–	100	μA

Notes

1. Value measured without influence of external circuitry.
2. Or not connected.
3. The signal amplitude of the colour difference signals (R-Y) and (B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
4. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

APPLICATION INFORMATION

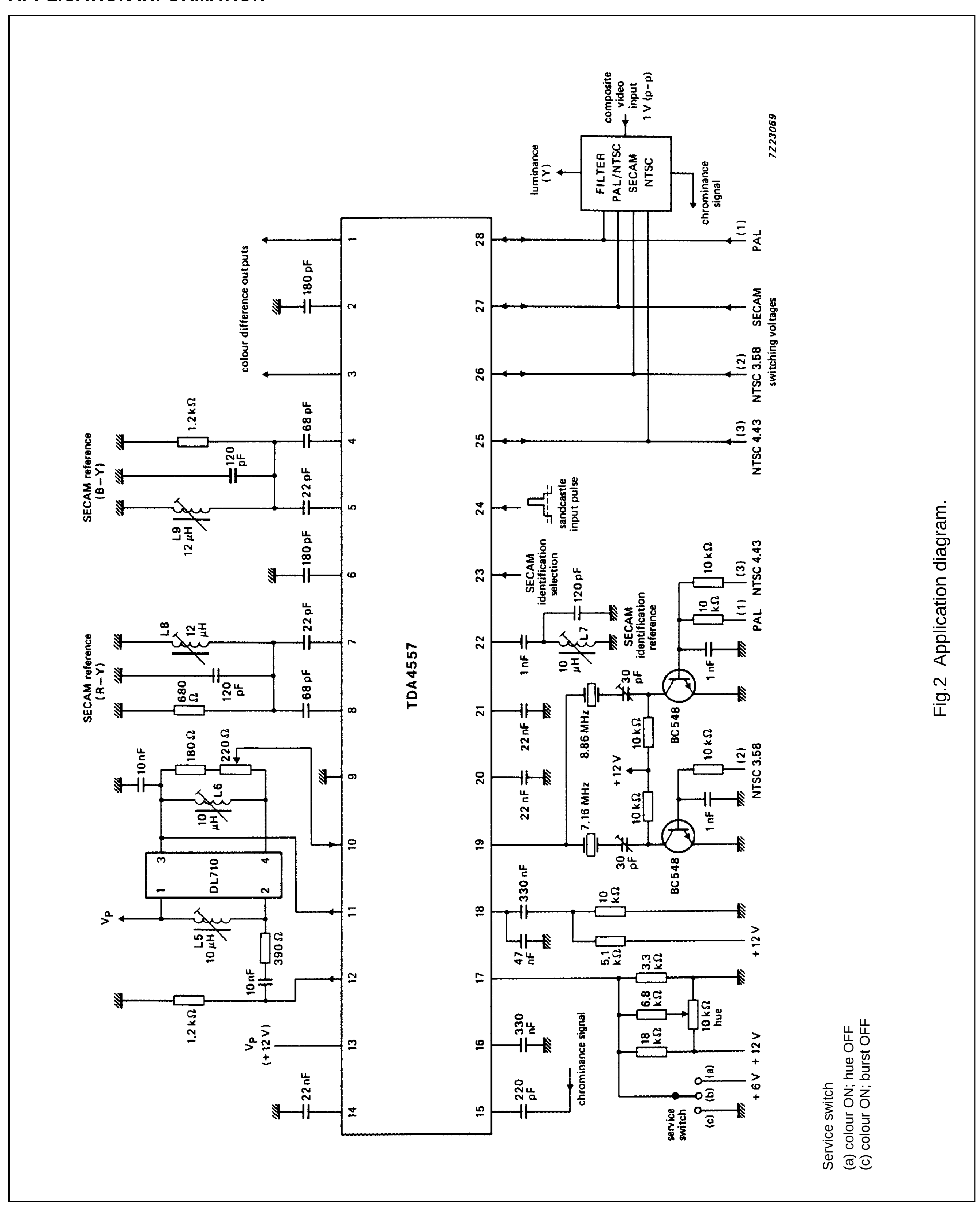
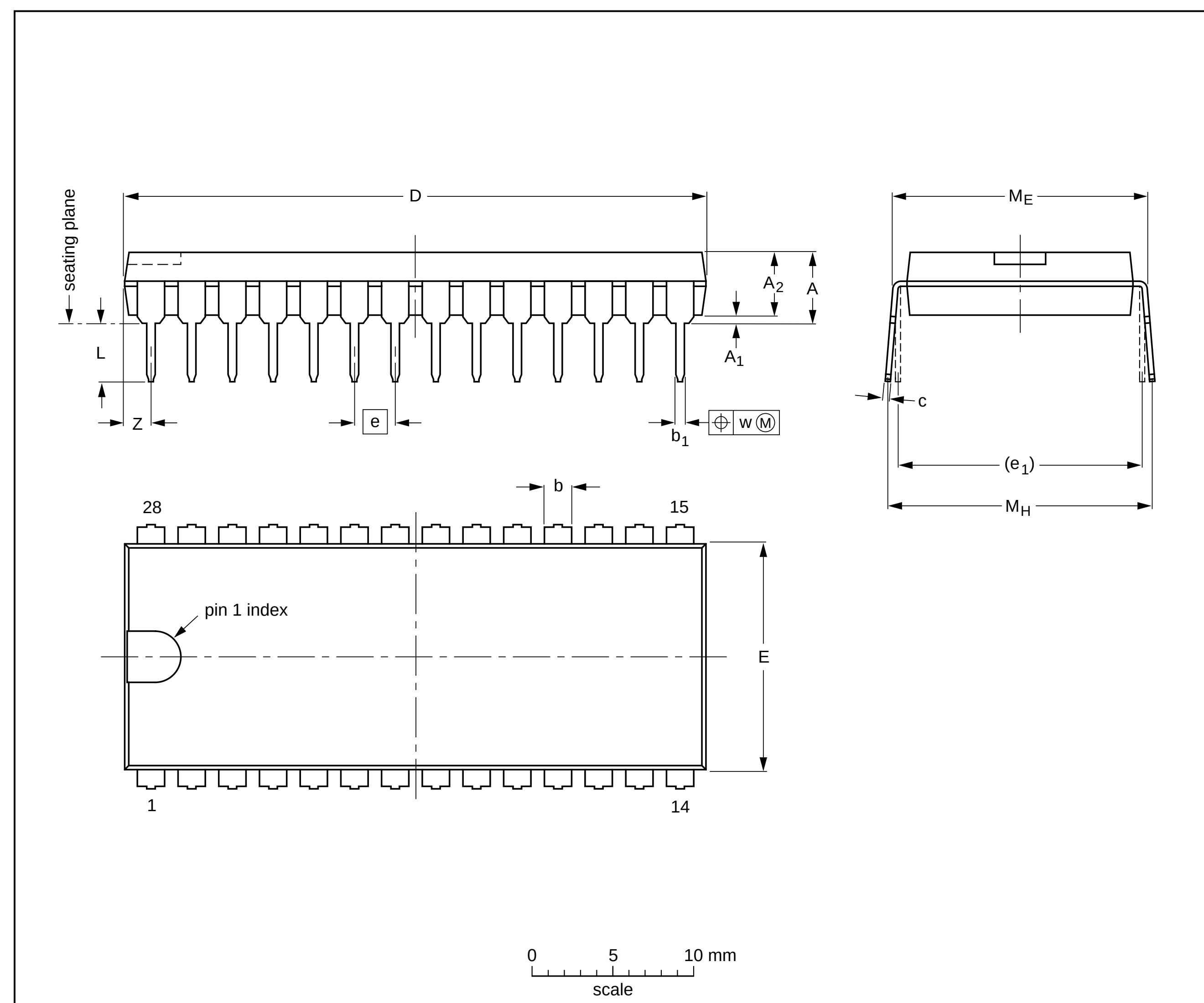


Fig.2 Application diagram.

PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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